1385DX
12.5 Gbps 1:8 Demultiplexer with Latched Comparator Input
Data Sheet

Applications

- Broadband test and measurement
- Automatic Test Equipment (ATE)
- Military/Aerospace Instrumentation
- Broadband Digital Cross-Connects

Features

- 1:8 DEMUX (to 12.5 Gbps)
- High-sensitivity latched comparator input
- Front-end bandwidth: 14 GHz typical
- Clock rates of DC to 12.5 GHz typical
- Differential, selectable-rate output clock, including half-rate
- Automatic synchronization of multiple 1385DX demultiplexers
- Low power consumption: 1.5 W typical
- Differential CML I/O with common mode adjust
- Single, +3.3 V power supply
- Available in 8x8 mm QFN

Description

The 1385DX is a broadband 1:8 demultiplexer (DEMUX) with a sensitive latched comparator input operating at bit rates from DC to 12.5 Gbps. Its serial data input features a very sensitive, low-hysteresis latched comparator front-end with an analog bandwidth of 14 GHz. The front end has specifications that are similar to the Inphi 13607CP latched comparator.

The 1385DX accepts a single external clock at up to 12.5 GHz that strobes the input signal into the latched comparator. The clocks used for demultiplexing the input are generated internally.

The 1385DX’s output clock frequency can be either 1/8th that of the input clock (full-rate mode) or 1/16th (half-rate mode) as determined by the CLKSEL input.

The 1385DX includes a synchronization circuit that allows two or more DEMUXs to be automatically synchronized. This is achieved in a master/slave mode in which the slave DEMUX synchronizes to a signal (CK16) from the master. Synchronization occurs within at most 272 periods of the input clock.

The high-speed data and clock I/O use current mode logic (CML) buffers and are back-terminated on chip. A separate power supply (VCCO) to the output buffers allows the output common mode voltage to be set as low as 1.7 V. Control inputs are low-voltage CMOS/TTL.

The 1385DX operates from standard +3.3 V power supplies. It is available in an 8x8 mm QFN package. Evaluation boards are also available.
Figure 1. Block diagram. Not all connections are shown, and, though the block diagram does not show it, many of the I/O are differential.
Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the “Operating Conditions” and “Electrical Specifications” of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Power Supply Level (V\text{CCD}) (^1)</td>
<td>-0.5</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>Analog Power Supply Level (V\text{CCA}) (^1)</td>
<td>-0.5</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>Output Buffer Power Supply Level (V\text{CCO}) (^1)</td>
<td>-0.5</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>Power Supply Difference (Digital to Analog)</td>
<td>V\text{CCD} - V\text{CCA}</td>
<td>--</td>
<td>0.6</td>
</tr>
<tr>
<td>Power Supply Difference (Digital to Output) V\text{CCD} - V\text{CCO}</td>
<td>-0.6</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>Ground difference (Digital to Analog)</td>
<td>GND - GNDA</td>
<td>--</td>
<td>0.6</td>
</tr>
<tr>
<td>Data Input Signals V\text{CCA} - 2</td>
<td>V\text{CCA} + 0.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Clock Input Signals V\text{CCD} - 2</td>
<td>V\text{CCD} + 0.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Control Inputs -0.5 V\text{CCD} + 0.6 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data and CKOUT Outputs -0.5 V\text{CCD} + 1.0 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CK16 Outputs -0.5 V\text{CCD} + 1.0 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Frequency LVCMOS outputs -0.5 V\text{CCD} + 1.0 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Case Temperature -55 +125 °C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shipping/Storage Temperature -55 +125 °C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Humidity 0 100 %</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Protection – Data Inputs: INP, INN (Human Body Model) 350 -- V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Protection – All other Input and Output pins (HBM) 500 -- V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Protection – Power Supplies (HBM) 500 -- V</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Note:

\(^1\) The Analog power supply (V\text{CCA}) and Digital supply (V\text{CCD}) should be connected together on the board.

\(^2\) The Analog ground (GNDA) and Digital ground (GND) should be connected together on the board.
### Operating Conditions: Supply and Environmental Limits

Performance specifications are guaranteed provided that the 1385DX is operated within the power supply and environmental specifications provided in this table.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog and Digital Power Supply Level 1,2</td>
<td>V&lt;sub&gt;CCDA&lt;/sub&gt;</td>
<td>± 5 % Tolerance</td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>Output Power Supply Level</td>
<td>V&lt;sub&gt;CCO&lt;/sub&gt;</td>
<td></td>
<td>1.7</td>
<td>1.8</td>
<td>3.5</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature (Case)</td>
<td>T&lt;sub&gt;C&lt;/sub&gt;</td>
<td></td>
<td>-40</td>
<td>---</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

Notes:
1. Connect the Analog power supply (V<sub>CCA</sub>) and Digital supply (V<sub>CCD</sub>) together (referred to as V<sub>CCDA</sub>).
2. Connect the Analog ground (GNDA) and Digital ground (GND) together.

### Supply Currents and Power Dissipation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Current (Analog + Digital)</td>
<td>I&lt;sub&gt;CCDA&lt;/sub&gt;</td>
<td>Sync enabled</td>
<td>---</td>
<td>400</td>
<td>460</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sync disabled</td>
<td>---</td>
<td>330</td>
<td>---</td>
<td>mA</td>
</tr>
<tr>
<td>Output Power Supply Current</td>
<td>I&lt;sub&gt;CCO&lt;/sub&gt;</td>
<td></td>
<td>---</td>
<td>80</td>
<td>---</td>
<td>mA</td>
</tr>
<tr>
<td>On-Chip Power Dissipation</td>
<td>P&lt;sub&gt;D&lt;/sub&gt;</td>
<td>Sync enabled</td>
<td>---</td>
<td>1.45</td>
<td>1.95</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sync disabled</td>
<td>---</td>
<td>1.25</td>
<td>---</td>
<td>W</td>
</tr>
</tbody>
</table>
# Input Electrical Specifications

**WARNING** – To prevent damage to the part:
- DC power must be turned off prior to connecting or disconnecting any cables.

Specifications guaranteed when the part is operated within the specified operating conditions.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs, Data (Analog): INp and INn</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input High Level</td>
<td>( V_{IH} )</td>
<td>( V_{CCA} - 0.5 )</td>
<td>---</td>
<td>( V_{CCA} + 0.3 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Low Level</td>
<td>( V_{IL} )</td>
<td>( V_{CCA} - 0.8 )</td>
<td>---</td>
<td>( V_{CCA} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Amplitude(^1,2)</td>
<td>( V_{INpp} )</td>
<td>Differential peak-to-peak</td>
<td>See Note #1</td>
<td>---</td>
<td>1200</td>
<td>mVpp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single-ended peak-to-peak</td>
<td>See Note #1</td>
<td>---</td>
<td>700</td>
<td>mVpp</td>
</tr>
<tr>
<td>DC Input Resistance</td>
<td>( R_{IN} )</td>
<td>Input to ( V_{CCA} )</td>
<td>---</td>
<td>62.5</td>
<td>---</td>
<td>Ω</td>
</tr>
<tr>
<td>Input Analog Bandwidth (3 dB)</td>
<td>( BW_{IN} )</td>
<td></td>
<td>---</td>
<td>14</td>
<td>---</td>
<td>GHz</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>( RL_{IN} )</td>
<td>( f &lt; 6.25 \text{ GHz} )</td>
<td>---</td>
<td>12</td>
<td>---</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f = 12.5 \text{ GHz} )</td>
<td>---</td>
<td>8</td>
<td>---</td>
<td>dB</td>
</tr>
<tr>
<td>Inputs, Clocks (CML): CLKINp, CLKINn, SCLK1p, SCLK1n, SCLK2p, SCLK2n</td>
<td></td>
<td>( f &lt; 6.25 \text{ GHz} )</td>
<td>---</td>
<td>1200</td>
<td>---</td>
<td>mVpp</td>
</tr>
<tr>
<td>CLKIN Input Amplitude(^3)</td>
<td>( V_{CLKpp} )</td>
<td>Differential peak-to-peak</td>
<td>400</td>
<td>---</td>
<td>1200</td>
<td>mVpp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single-ended peak-to-peak</td>
<td>400</td>
<td>---</td>
<td>700</td>
<td>mVpp</td>
</tr>
<tr>
<td>SCLK Input Amplitude(^3)</td>
<td>( V_{SCLKpp} )</td>
<td>Differential peak-to-peak</td>
<td>200</td>
<td>---</td>
<td>1200</td>
<td>mVpp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single-ended peak-to-peak</td>
<td>200</td>
<td>---</td>
<td>700</td>
<td>mVpp</td>
</tr>
<tr>
<td>DC Input Resistance</td>
<td>( R_{CLKIN} )</td>
<td>Input to ( V_{CCD} )</td>
<td>---</td>
<td>50</td>
<td>---</td>
<td>Ω</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>( S_{MIN} )</td>
<td>At the zero crossing</td>
<td>1</td>
<td>---</td>
<td>---</td>
<td>V/ns</td>
</tr>
<tr>
<td>CLKIN Input Return Loss</td>
<td>( RL_{CLKIN} )</td>
<td>( f &lt; 6.25 \text{ GHz} )</td>
<td>---</td>
<td>10</td>
<td>---</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f = 12.5 \text{ GHz} )</td>
<td>---</td>
<td>7</td>
<td>---</td>
<td>dB</td>
</tr>
<tr>
<td>Maximum CLKIN Frequency</td>
<td>( f_{CLKIN,MAX} )</td>
<td>Differential, square wave clock or Single-ended, sine wave clock</td>
<td>12.5</td>
<td>---</td>
<td>---</td>
<td>GHz</td>
</tr>
<tr>
<td>Minimum CLKIN Frequency</td>
<td>( f_{CLKIN,MIN} )</td>
<td>Differential, square wave clock</td>
<td>---</td>
<td>0.2</td>
<td>---</td>
<td>GHz</td>
</tr>
<tr>
<td>CLKIN Duty Cycle</td>
<td>( DC_{CLKIN} )</td>
<td></td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>Maximum operating Frequency of Synchronization Circuit(^4)</td>
<td></td>
<td></td>
<td>(see note 4)</td>
<td>12.5</td>
<td>---</td>
<td>GHz</td>
</tr>
</tbody>
</table>

Notes:
1. When operating the 1385DX as a purely digital Demultiplexer (serial-to-parallel converter), that is driving the Data inputs with a digital, serial data stream, the minimum input amplitude allowed is 400 mVpp (differential) or 400 mVpp (single-ended). When operating the 1385DX as a mono-bit receiver (latched comparator with an 8-bit demultiplexed output bus), the minimum input amplitude allowed is dependent on the hysteresis, which is data rate dependent (see section on Hysteresis, page 8).
2. Data (Analog) and clock input amplitudes < 300 mVpp may cause part to fail the following AC electrical specifications: Deterministic Jitter, Random Jitter, and Clock to Data Output Delay.
3. Input clocks have internal DC blocks. For that reason, input DC levels are not stated.
4. Assumes that the propagation delay of the CK16 output (of the master 1385DX) to the SCLK2 input (of the slave 1385DX) is < 500 ps. See “Synchronization Circuit Operation.”
Input Specifications

**WARNING** – To prevent damage to the part:
- DC power must be turned off prior to connecting or disconnecting any cables.

Inputs, Low Frequency Control (LVCMOS/LVTTL): SYNEN, MANRST, CLKSEL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input High Level</td>
<td>V_{IH}</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Low Level</td>
<td>V_{IL}</td>
<td>GND</td>
<td></td>
<td></td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Input Current</td>
<td>I_{IN}</td>
<td>V_{IL} &lt; Input Voltage &lt; V_{IH}</td>
<td>-1</td>
<td></td>
<td>0.1</td>
<td>mA</td>
</tr>
<tr>
<td>Input DC Resistance</td>
<td>R_{CNTL}</td>
<td>Input to V_{CC}</td>
<td>---</td>
<td>5</td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

Output Electrical Specifications

**WARNING** – To prevent damage to the part:
- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outputs, Data (CML): D0p...D7p, D0n...D7n</td>
<td>V_{OH}</td>
<td>V_{CCD} referenced</td>
<td>---</td>
<td>-10</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>V_{OL}</td>
<td>V_{CCD} referenced</td>
<td>---</td>
<td>-250</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>V_{CM}</td>
<td>V_{CCD} referenced</td>
<td>---</td>
<td>-125</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>V_{OUTPP}</td>
<td>Differential peak-to-peak</td>
<td>---</td>
<td>500</td>
<td></td>
<td>mVpp</td>
</tr>
<tr>
<td></td>
<td>R_{OUT}</td>
<td>Output to V_{CCO}</td>
<td>---</td>
<td>65</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Rise and Fall Times</td>
<td>t_{R}/t_{F}</td>
<td>20% to 80%</td>
<td>---</td>
<td>110</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>Deterministic Jitter</td>
<td>J_{D}</td>
<td>Peak-to-peak</td>
<td></td>
<td></td>
<td>15</td>
<td>ps</td>
</tr>
</tbody>
</table>

Output Clocks (CML): CKOUTp, CKOUTn, CK16p, CK16n

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output High Level</td>
<td>V_{OH}</td>
<td>V_{CCD} (or V_{CCD}) referenced</td>
<td>---</td>
<td>-10</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Output Low Level</td>
<td>V_{OL}</td>
<td>V_{CCD} (or V_{CCD}) referenced</td>
<td>---</td>
<td>-250</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Output Common Mode</td>
<td>V_{CM}</td>
<td>V_{CCD} (or V_{CCD}) referenced</td>
<td>---</td>
<td>-125</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Output Amplitude</td>
<td>V_{OUTPP}</td>
<td>Differential peak-to-peak</td>
<td>---</td>
<td>500</td>
<td></td>
<td>mVpp</td>
</tr>
<tr>
<td>Output DC Resistance</td>
<td>R_{OUT}</td>
<td>Output to V_{CCO}</td>
<td>---</td>
<td>65</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Rise and Fall Times</td>
<td>t_{R}/t_{F}</td>
<td>20% to 80%</td>
<td>---</td>
<td>100</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>Random Jitter</td>
<td>J_{R}</td>
<td>RMS, using 1010... pattern</td>
<td>---</td>
<td>2</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td></td>
<td></td>
<td>---</td>
<td>50</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Output Data Eye Center to</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CKOUT Rising/Falling Edge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>Output (LVCMOS/LVTTL): SYNC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output High Level</td>
<td>V_{OH}</td>
<td></td>
<td>2.6</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Output Low Level</td>
<td>V_{OL}</td>
<td>GND</td>
<td></td>
<td></td>
<td>0.4</td>
<td>mV</td>
</tr>
</tbody>
</table>
Output Electrical Specifications (cont’d.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Low Output Current</td>
<td>I_{OUT}</td>
<td>Current into SYNC pad</td>
<td>3</td>
<td>---</td>
<td>---</td>
<td>mA</td>
</tr>
<tr>
<td>Output DC Resistance</td>
<td>R_{OUT}</td>
<td>Output to VCC</td>
<td>---</td>
<td>5</td>
<td>---</td>
<td>kΩ</td>
</tr>
<tr>
<td>Rise Time</td>
<td>t_{R}</td>
<td>20% to 80%, C_{L} = 1 pF</td>
<td>---</td>
<td>3.5</td>
<td>---</td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time</td>
<td>t_{F}</td>
<td>80% to 20%, C_{L} = 1 pF</td>
<td>---</td>
<td>0.05</td>
<td>---</td>
<td>ns</td>
</tr>
<tr>
<td>SYNC Pulse Duration</td>
<td></td>
<td>SYNC &lt; 0.8 V</td>
<td>32</td>
<td>---</td>
<td>---</td>
<td>cycles</td>
</tr>
<tr>
<td>Lock Time</td>
<td>t_{LOCK}</td>
<td></td>
<td>---</td>
<td>---</td>
<td>272</td>
<td>cycles</td>
</tr>
<tr>
<td>Detect Time</td>
<td>t_{DET}</td>
<td></td>
<td>---</td>
<td>---</td>
<td>32</td>
<td>cycles</td>
</tr>
</tbody>
</table>

Notes:
1. Data Outputs, both DxP and DxN, must be terminated. If CKOUT or CK16 is used single-endedly, the complementary output must be terminated. All terminations should be 50 ohms to V_{CCD} (V_{CDD} for CK16) and can be either DC or AC coupled.
2. It should be noted that because the random and deterministic jitter of this part is "in the noise" of the measurement equipment and techniques used, these specifications are conservative. The deterministic jitter (JD) specified above is actually the peak-to-peak total jitter measured using a 2^{31}-1 PRBS data pattern. The random jitter (JR) is the RMS jitter measured on a clock. Neither the random nor deterministic jitter of the source and measurement equipment was removed from the measurement data used to derive the above specifications.
3. The rising and falling edges of the CKOUT clock output occur near the center of the output data eye, independent of the CLKSEL setting and the input data rate.
4. This is the maximum current that the SYNC output can sink while maintaining a logic low voltage level.
5. External 5 kΩ pull-up resistor to V_{CCD} is assumed.
6. The external load capacitance (C_{L}) connected to the SYNC output pin is assumed to be 1 pF. The actual rise and fall times will be proportional to the actual C_{L}.
7. Following startup or an upset event, SYNC will be asserted after this number of input clock cycles, indicating that the SCLK1 and SCLK2 clocks are in phase (reference figure on page 14).
8. Following an upset event, SYNC will be de-asserted after this number of input clock cycles, to indicate that the SCLK1 and SCLK2 clocks are out of phase (reference figure on page 14).
Hysteresis Characteristics

Figure 2. Expected, analog input (IN+) typical DC hysteresis of the 1385DX’s front-end comparator; These expected data were taken from the 25706CP data sheet. The 25706CP and 1385DX have the same front end. For this measurement, the offset voltage was calculated from the swept data by taking the average of the threshold for the positive and negative sweep. The difference between the thresholds is the hysteresis.

Figure 3. Expected, Analog input (IN+) thermal hysteresis of the 1385DX’s front-end comparator is shown as a function of input soak time in μs (and equivalent data rate in Mb/s); These expected data were taken from the 25706CP data sheet. The 25706CP and 1385DX have the same front end. The Input data pattern used was a 1010… square wave at the specified data rates. The Clock frequency was set to 1 GHz.

CKOUT Mode of Operation (CLKSEL pin)

The 1385DX has a CKOUT mode of operation selected by the CLKSEL input as described in the following table. The CLKSEL input is a low-voltage CMOS/TTL input. Note that if this input is left unconnected, an on-chip resistor sets the default state of the chip to half-rate output clock (CKOUT).

Table 1. Description of CKOUT mode of operation as governed by the CLKSEL input.

<table>
<thead>
<tr>
<th>CLKSEL</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1:8 DEMUX, normal mode. The CKOUT frequency is 1/8 of the input clock frequency.</td>
</tr>
<tr>
<td>1*</td>
<td>1:8 DEMUX, half-rate mode. The CKOUT frequency is 1/16 of the input clock frequency.</td>
</tr>
</tbody>
</table>

* Default state, set by an on-chip pull-up resistor.
**MANRST**

The manual reset (MANRST) feature may be used to synchronize two 1385DXs that are located far apart, where the CK16 to SCLK transmission line delay is greater than 500 ps. Manual synchronization is achieved by asserting the MANRST input of one of the two 1385DXs until the output clocks (CKOUT or CK16) of the two demultiplexers are in phase. Reset is asserted when the MANRST pin is held to a logic low. During normal operation MANRST should be left open or held to a logic high state. Asserting the MANRST input results in an asynchronous reset of the counter that generates the various clocks used in the demultiplexer. The MANRST is a slow, LVCMOS/LVTTL input. When reset, the counter will come up in one of sixteen states. So the probability that the counter of one 1385DX will be in the same state as the counter on another 1385DX is 0.0625. Therefore, synchronization of two 1385DXs by this method is a stochastic process requiring, on average, 16 attempts.

**Synchronization Circuit Operation**

The SYNEN enable input controls whether the synchronization circuit is enabled (operational) or not. If not enabled, the synchronization circuit is turned off to save power. The SYNEN input is a low-voltage CMOS/TTL input with an on-chip pull-up resistor so that the synchronization circuit defaults to the enabled state.

**Important:** When the synchronization circuit is enabled, valid signals must be present at the SCLK1 and SCLK2 inputs.

<table>
<thead>
<tr>
<th>SYNEN</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1*</td>
<td>Synchronization circuit is enabled. When enabled, valid signals must be present at the SCLK1 and SCLK2 inputs.</td>
</tr>
<tr>
<td>0</td>
<td>Synchronization circuit is disabled and powered down. The SYNEN input of the master DEMUX should be disabled.</td>
</tr>
</tbody>
</table>

*Default state, set by an on-chip pull-up resistor.*

The CK16 output clock is used to automatically synchronize the counters on two demultiplexers. The CK16 frequency is always 1/16 of the input clock frequency. When the counters are synchronized, the CK16 and CKOUT clock outputs of the slave 1385DX will be in phase with those of the master 1385DX. (Note: the CK16 outputs and SCLK1 and SCLK2 inputs are referenced to V\textsubscript{CCD}. The CKOUT outputs are referenced to V\textsubscript{CCO}).

Two 1385DX DEMUXs can be synchronized by connecting them as shown in Figure 4. For simplicity, only the DEMUX clock inputs and outputs are shown. The upper DEMUX in Figure 4 is the master and the lower one is the slave. The clock inputs (CLKIN) to the two DEMUXs should be routed in such a way as to ensure that the CLKIN inputs of the two DEMUXs are in phase, to within 10 ps. One way to accomplish this is to use an Inphi 13617CF 1:2 clock fan-out with outputs routed through equal-length transmission lines (C1 and C2). The CK16 clock from the master is routed to the SCLK2 input of the slave through 50-ohm transmission line (A). The CK16 clock output of the slave DEMUX is routed to the slave’s SCLK1 input through another 50-ohm transmission line (B), whose length is equal to that of line (A). The electrical lengths of transmission lines A and B should be matched to within 10 ps. Since the two CK16 clock outputs are generated by the counters in the two DEMUXs, the DEMUXs will be synchronized when the SCLK1 and SCLK2 inputs of the slave DEMUX are in phase. The synchronization circuit on the slave will automatically adjust the phase of its CK16 output until the phases of the two signals at its SCLK1 and SCLK2 inputs are within 20 ps. Synchronization will occur in a maximum of 272 input clock cycles. Upon synchronization, the phase of the master and the slave CKOUT output clocks will be phase matched to within 10ps, as determined by the matching of the CLKIN transmission lines.
Synchronization Circuit Operation (cont’d.)

![Diagram](image)

**Figure 4.** Block diagram showing how to synchronize two DEMUXs; Only clock inputs and outputs are shown for simplicity.

Note the following:

1. The SYNEN input of the Master DEMUX should be driven with a LVTTL/CMOS logic low so that its synchronization circuit is disabled.
2. The CLKin inputs are AC coupled on chip and should always be terminated, even if not used. (See Clock input buffer schematic on Figure 9.)
3. It is not necessary to drive the SCLK1 and SCLK2 inputs differentially.
4. The SCLK inputs are AC coupled on chip, so if, for example, the SCLK1 input is driven single-endedly, the SCLK1B input may be left floating. However, if, in this example, the SCLK1B input were connected to a transmission line, it is recommended that the transmission line have a proper termination at its other end.
5. Unused CK16 outputs should be terminated with 50 Ω resistors to V CCD only if the unused output is bonded to a transmission line. Otherwise the output port may be un-terminated.
6. The CK16 outputs are referenced to V CCD. The CKOUT outputs are referenced to V CCO.
7. The SCLK1 and SCLK2 inputs are referenced to V CCD.

Once the CKOUT outputs of two DEMUXs are in phase (again, to within 10 ps as determined by the matching of the CLKin transmission lines), the SYNC output will be asserted. The SYNC output is a low frequency LVTTL/CMOS signal. Note that if the SYNEN input is inactive (synchronization circuit is disabled and powered down), the SYNC output is indeterminate.

**Synchronization of More than Two DEMUXs**

Several DEMUXs can be synchronized by “daisy chaining” as shown in Figure 5. The phases of all input clocks (CLKin) must be the same, to within 10 ps. The SCLK transmission lines of adjacent DEMUXs must be matched to within 10 ps as described in the previous section. Synchronization of a “daisy chained” configuration will occur in a maximum of (N-1) times 272 input clock cycles, where N is the number of “daisy chained” DEMUXs. Note that the scheme alternately uses the true and complementary CK16 outputs so that the phase difference of the signals present at a particular demultiplexer’s SCLK inputs is zero when the demultiplexers are synchronized. Also note that 1:2 differential clock fan-outs are used with true and complementary clocks driving true and complementary clock inputs on adjacent DEMUXs. It is recommended that Inphi 13617CF 1:2 clock fan-outs be used for clock distribution to the DEMUXs.
Synchronization of More than Two DEMUXs (cont’d.)

Figure 5. Block diagram showing synchronization of 6 DEMUXs.

Note the following:
1. The CLKin inputs are AC coupled on chip and should always be terminated, even if not used.
2. The SCLK inputs are AC coupled on chip, thereby eliminating the need to terminate the unused SCLK input ports provided that they are not connected to external transmission lines. Unused SCLK inputs do not need to be terminated since this frequency at this input is 1/16th of fCLKin. If, however, the unused input ports are connected to transmission lines, it is recommended that these transmission lines be properly terminated at the other ends. Doing so will decrease the possibility that RF energy that is somehow coupled to these lines will interfere with the operation of the synchronization circuit.
3. Unused CK16 output ports should be terminated with 50 Ω resistors to VCC only if the unused output is connected to a transmission line. Otherwise the output port may be un-terminated, since a back-termination is present on-chip.
**Timing Information**

**Half rate clock mode of operation.** CLKSEL = 1. CKOUT frequency = 1/16th of input clock (CLKin) frequency.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Data Edge to Clock Edge and Clock Edge to Data Edge Time</td>
<td>tDC, tCD</td>
<td>---</td>
<td>(data period)/2 + 10</td>
<td>---</td>
<td>ps</td>
</tr>
<tr>
<td>Input Clock to Data Time</td>
<td>tPD</td>
<td>---</td>
<td>8</td>
<td>---</td>
<td>input clocks</td>
</tr>
</tbody>
</table>
**Timing Information (cont’d.)**

**Full rate clock mode of operation.** CLKSEL = 0. CKOUT frequency = 1/8<sup>th</sup> of input clock (CLKin) frequency.

![Diagram showing timing information](diagram.png)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Edge to Clock Rising Edge&lt;sup&gt;1&lt;/sup&gt;</td>
<td>tDC</td>
<td>---</td>
<td>7/16&lt;sup&gt;th&lt;/sup&gt; of data period</td>
<td>---</td>
<td>ps</td>
</tr>
<tr>
<td>Input Clock to Data Time&lt;sup&gt;1&lt;/sup&gt;</td>
<td>tPD</td>
<td>---</td>
<td>8</td>
<td>---</td>
<td>input clocks</td>
</tr>
</tbody>
</table>

Note:

<sup>1</sup> The rising/falling edge of the output clock will occur in the center of the output data eye.
Timing Information (cont’d.)

Lock Timing for the Master and Slave Configuration in Figures 6 & 7.
Lock timing is independent of the state of the CLKSEL input.

Detect Timing for the Master and Slave Configuration in Figures 6 & 7.
Detect timing is independent of the state of the CLKSEL input.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lock Time¹</td>
<td>( t_{\text{lock}} )</td>
<td>---</td>
<td>---</td>
<td>272</td>
<td>input clocks</td>
</tr>
<tr>
<td>Detect Time¹</td>
<td>( t_{\text{det}} )</td>
<td>---</td>
<td>---</td>
<td>32</td>
<td>input clocks</td>
</tr>
</tbody>
</table>

Note:
¹ Since two clocks, a master and a slave, may startup in or be forced into (due to an upset event) one of sixteen random states, only the worst-case lock times and detect times are presented here.
Typical Operating Characteristics

Figure 6. CKOUT & DOUTp data eye (AC coupled); Source is 12.1 Gbps 2^−1 PRBS pattern (scope view is 50 mV/div, 200 ps/div).

Typical S-Parameter Characteristics

Figure 7. S11 amplitude of INp and INn

Figure 8. S11 amplitude of Clock Input CLKIN
I/O and Power Supply Equivalent Circuits

On-Chip Input AC Coupling for CLKIN, SCLK1, SCLK2

- CLKIN to VCC: 50 Ω, 1 pF, 160 MHz Hi-Pass
- SCLK to VCC: 50 Ω, 1 pF, 32 MHz Hi-Pass

Figure 9. Equivalent circuit diagrams of the CLKIN and SCLK clock inputs

Analog/Data Inputs (INp & INn) and Low Speed Outputs

- IN to VCCA: 63 Ω
- IN to GND
- VCCA to IN
- VCCO to Out
- Out to GND
- 65 Ω

Figure 10. Equivalent circuit diagrams of data inputs and outputs

Power Domain Coupling and ESD

- VCCA: 3.3 V Crowbar
- GND
- VCCD: 3.3 V Crowbar
- VCCO: 3.3 V Crowbar
- Front-End: Diodes ~ 700 mV
- VBE multiplier ~ 1.8 V
- Out Buffers

Figure 11. Equivalent diagram of the power supply coupling and ESD protection
QFN Package Outline Drawing

Package Info:
JEDEC Standard Document MO-220, Variation VLL0-5

Dimension Unit: mm
QFN Pin Assignment

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin</th>
<th>Description</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>INp</td>
<td>7</td>
<td>Non-inverting data input: On-chip 62.5 Ω termination to VCCA provided. Inputs can be DC-coupled differential or AC-coupled single-ended or differential. When driven single-endedly, the unused input may be left floating. External AC coupling required for ground reference.</td>
<td>High Frequency Data Input</td>
</tr>
<tr>
<td>INn</td>
<td>8</td>
<td>Inverting data complimenting INp.</td>
<td>High Frequency Data Input</td>
</tr>
<tr>
<td>CLKINp</td>
<td>16</td>
<td>Non-inverting clock Input: On-chip 50 Ω termination to VCCD provided. Integrated DC blocks included with low frequency 3 dB corner of 160 MHz. May be driven differentially or single-endedly. When driven single-endedly, the unused input may be left floating.</td>
<td>Clock Input</td>
</tr>
<tr>
<td>CLKINn</td>
<td>17</td>
<td>Inverting clock Input corresponding to CLKINp.</td>
<td>Clock Input</td>
</tr>
<tr>
<td>D0p, D1p, D2p, D3p, D4p, D5p, D6p, D7p</td>
<td>46, 41, 39, 37, 33, 31, 29, 25</td>
<td>Non-inverting, low-speed, data outputs. Each output is back-terminated on-chip to VCCO with 65 Ω. Unused outputs should be terminated with 50 Ω to VCCO.</td>
<td>Data Outputs</td>
</tr>
<tr>
<td>D0n, D1n, D2n, D3n, D4n, D5n, D6n, D7n</td>
<td>47, 42, 40, 38, 34, 32, 30, 26,</td>
<td>Inverting, low-speed, data outputs complimenting D[0:7]p.</td>
<td>Data Outputs</td>
</tr>
<tr>
<td>CKOUTp</td>
<td>22</td>
<td>Non-inverting, VCCO referenced clock outputs. Each output is back-terminated on-chip to VCCO with 65 Ω. Unused outputs should be terminated with 50 Ω to VCCO.</td>
<td>Clock Output</td>
</tr>
<tr>
<td>CKOUTn</td>
<td>23</td>
<td>Inverting, VCCO referenced clock output complimenting CKOUTp.</td>
<td>Clock Output</td>
</tr>
<tr>
<td>CK16p</td>
<td>19</td>
<td>Non-inverting, VCCD referenced clock output. To be used for synchronizing two 1385DXs. Each output is back-terminated on-chip to VCCD with 65 Ω. Unused outputs should be terminated with 50 Ω to VCCD only if the unused output is bonded to a transmission line. Otherwise the output port may be left floating.</td>
<td>Clock Output</td>
</tr>
</tbody>
</table>
## QFN Pin Assignment (cont’d.)

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin</th>
<th>Description</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CK16n</td>
<td>20</td>
<td>Inverting, V_{CCD} referenced clock output complimenting CK16p.</td>
<td>Clock Output</td>
</tr>
<tr>
<td>SCLK1p,</td>
<td>55,</td>
<td>Non-inverting synchronization clock inputs: On-chip 50 Ω termination to V_{CCD}</td>
<td>Synchronization Clock Inputs</td>
</tr>
<tr>
<td>SCLK2p</td>
<td>52</td>
<td>provided. Integrated DC blocks included with low frequency 3 dB corner of 32 MHz. May be driven differentially or single-endedly. When driven single-endedly, the unused input may be left floating.</td>
<td></td>
</tr>
<tr>
<td>SCLK1n,</td>
<td>54,</td>
<td>Inverting synchronization clock inputs corresponding to SCLK[1:2]p.</td>
<td>Synchronization Clock Inputs</td>
</tr>
<tr>
<td>SCLK2n</td>
<td>51</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NC</td>
<td>13</td>
<td>No Connect. not internally connected to the die</td>
<td></td>
</tr>
<tr>
<td>CLKSEL</td>
<td>12</td>
<td>Clock mode select. If left unconnected or driven with a logic high, CKOUTp &amp; CKOUTn are 1/16 the input clock frequency. If driven with a logic low, CKOUTp &amp; CKOUTn are 1/8 the input clock frequency.</td>
<td>LVCMOS Input</td>
</tr>
<tr>
<td>SYNEN</td>
<td>2</td>
<td>Synchronization enable. Enables the on-chip synchronization circuit. If left unconnected or driven with a logic high, the synchronization circuit is enabled. See Synchronization circuit section in this specification for details. If driven with a logic low, the synchronization circuit is powered down.</td>
<td>LVCMOS Input</td>
</tr>
<tr>
<td>MANRST</td>
<td>3</td>
<td>Manual Reset. Toggling this pin performs an asynchronous reset of the counter that generates the on-chip clocks used to strobe the demultiplexers. Counter resets when MANRST is low. The state to which the counter is reset is random. MANRST is for use in synchronizing two demultiplexers that can’t be synchronized with the on-chip synchronization circuit because, for example, the two demultiplexers are located more than several inches from each other.</td>
<td>LVCMOS Input</td>
</tr>
<tr>
<td>SYNC</td>
<td>50</td>
<td>Synchronization Output. This pin is a valid LVTTL/LVCMOS logic high when the IC is synchronized with another 1385DX – i.e. when the SCLK1 and SCLK2 inputs, and therefore the master 1385DX and slave 1385DX CKOUT outputs, are in phase (to within several picoseconds). Connect with external 5 kΩ pull up to V_{CCDA}. See Synchronization circuit section in this specification for details.</td>
<td>LVCMOS Output</td>
</tr>
<tr>
<td>V_{CCA}</td>
<td>4,</td>
<td>Analog Power Supply. Provides power to the input latched comparator. Separate from V_{CCD} and V_{CCO} so as to improve sensitivity of the input. Connect to +3.3 V DC. Connect to +3.3 V DC.</td>
<td>Supply</td>
</tr>
<tr>
<td>V_{CCD}</td>
<td>1,</td>
<td>Digital Power Supply: Connect to +3.3 V DC.</td>
<td>Supply</td>
</tr>
<tr>
<td>V_{CCO}</td>
<td>28,</td>
<td>Power Supply for Output Buffers. May be connected to any potential between 1.8 V and 3.3 V.</td>
<td>Supply</td>
</tr>
<tr>
<td>GND</td>
<td>15,</td>
<td>Ground</td>
<td>Supply</td>
</tr>
<tr>
<td>GNDA</td>
<td>5,</td>
<td>Analog Ground</td>
<td>Supply</td>
</tr>
</tbody>
</table>
Order Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1385DX-S02QFN</td>
<td>12.5 Gbps 1:8 Demultiplexer with Latched Comparator Input (+3.3 V Supply) in QFN Package</td>
</tr>
<tr>
<td>1385DX-S02QFN-EVB</td>
<td>12.5 Gbps 1:8 Demultiplexer with Latched Comparator Input (+3.3 V Supply) in QFN Package on an Evaluation Board with SMA Connectors</td>
</tr>
</tbody>
</table>

Contact Information

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For each customer application, customer's technical experts must validate all parameters. Inphi Corporation reserves the right to change product specifications contained herein without prior notice. No liability is assumed as a result of the use or application of this product. No circuit patent licenses are implied. Contact Inphi Corporation’s marketing department for the latest information regarding this product.

Qualification Notification

⚠️ The 1385DX-S02 is fully qualified. Please contact Inphi for the qualification report.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi’s Standard Customer Purchase Order Terms and Conditions.

Version Updates

Version 1.0 (dated 2007-12-11):
Initial Release of 1385DX-S01QFN.

Version 1.0 to 2.0 (dated 2008-02-05):
1. Added Preliminary watermark to document.
2. Updated Features section (page 1):
   a. Typical power dissipation changed from 1.2 W to 1.5 W.
3. Updated Description section (page 1):
   a. Changed synchronization time from 152 to 272 clock periods.
4. Updated Operating Conditions: Supply and Environmental Limits
   a. Combined Digital and Analog supply levels (V_{CCDA}).
   b. Removed GNDA to GND levels difference parameter and its specs.
5. Updated Supply Current and Power Dissipation table (page 4):
   a. Combined analog and digital supply currents (I_{CCDA})
      i. Added 2 Conditions:
a. Sync enabled with typ spec = 400 mA and max spec = 460 mA
b. Sync disabled with typical specs = 330 mA
   ii. Max spec = 460 mA
b. Updated On-Chip Power dissipation parameter:
   i. Added 2 Conditions:
      1. Sync enabled with typ spec of 1.45 W and max spec of 1.95 W
      2. Sync disabled with typ spec of 1.25 W
6. Updated Input Electrical Specifications table (page 5):
   a. Updated Inputs, Data (Analog): INp and INn section:
      i. Clock and Data VIH and VIL: specs changed to be identical to the latched comparator:
         1. New specs: VIH min = VCCA -0.5 V; VIH max – VCCA +0.3 V.
            VIL min = VCCA – 0.8 V; VIL max = VCCA.
         2. Old specs:    VIH min = VCCA -0.1 V; VIH max – VCCA +0.3 V.
            VIL min = V CCA – 0.7 V; VIL max = VCCA – 0.125 V.
      ii. Added footnote to Input Amplitude parameter.
      iii. Removed min and max specs for DC Input Resistance parameter.
      iv. Removed min spec for Input Analog Bandwidth parameter.
      v. Removed Input Hysterisis (DC) parameter and its specs. (“Hysterisis Characteristics” on page 8 demonstrates Input Hysterisis performance.)
      vi. Removed Absolute Input Offset Voltage parameter and its specs.
      vii. Updated Input Return Loss parameter:
         1. Added two conditions with specifications
            a. f < 6.25 GHz
               i. Typ spec = 12 dB
            b. f = 12.5 GHz
               i. Typ spec = 8 dB
   b. Updated Inputs, Clocks (CML): CLKINp, CLKINn, SCLK1p, SCLK1n, SCLK2p, SCLK2n section:
      i. Removed Input High Level and Input Low Level parameters and specs, because input clock is AC coupled on chip.
      ii. Updated Input Amplitude parameter
         1. Created 2 parameters:
            a. Parameter name = “CLKIN Input Amplitude”
               i. Symbol = VCLKpp
               ii. Conditions
                  1. Differential peak-to-peak with min spec = 400 mVpp and max spec = 1200 mVpp
                  2. Single-ended peak-to-peak with min spec = 400 mVpp and max spec = 700 mVpp
            b. Parameter name = “SCLK Input Amplitude”
               i. Symbol = VSCLKpp
               ii. Conditions
                  1. Differential peak-to-peak with min spec = 200 mVpp and max spec = 1200 mVpp
                  2. Single-ended peak-to-peak with min spec = 200 mVpp and max spec = 700 mVpp
         2. Added footnote.
      iii. Removed min and max specs for DC Input Resistance parameter.
      iv. Updated Input Return Loss parameter:
         1. Changed parameter name from “Input Return Loss” to “CLKIN Input Return Loss”.
2. Added two conditions with specifications 
   a. \( f < 6.25 \text{ GHz} \) 
      i. Typ spec = 10 dB 
   b. \( f = 12.5 \text{ GHz} \) 
      i. Typ spec = 7 dB 

v. Updated Maximum CLKIN Frequency parameter: 
   1. Added “..or Single-ended, sine-wave clock” to Conditions 
   2. Changed minimum spec from 10 GHz to 12.5 GHz 
   3. Removed typical spec of 12.5GHz. 

vi. Updated Minimum CLKIN Frequency parameter: 
   1. Removed “..or Single-ended, sine-wave clock” from Conditions 

vii. Removed min and max specs for CLKIN duty cycle parameter 

viii. Removed the Clock to Data Input Isolation parameter and specs. 

ix. Removed CLKIN Setup and Hold Time parameter and its specs 

tax. Added Maximum Operating Frequency of Synchronization Circuit parameter with 
min spec = 12.5 GHz. 

xi. Updated Footnote # 1, by changing 500 mVpp to 400 mVpp within the note. 

7. Updated Input Specifications table (page 6): 
   a. Removed min and max specs for Input DC Resistance parameter. 

8. Removed the Input Return Loss Specifications section and renumbered the figures accordingly. 

9. Updated Output Electrical Specifications table (page 6): 
   a. Removed min and max specs for the following Data and Clock parameters: 
      i. Output High Level, 
      ii. Output Low Level 
      iii. Output Common Mode, 
      iv. Output Amplitude 
      v. Output DC Resistance 
   b. Updated Outputs, Data (CML): D0p..D7p, D0n..D7n section: 
      i. Updated Rise and Fall Times parameter: 
         1. Changed the typical spec from 75 ps to 110 ps. 
         2. Removed max spec. 
      ii. Updated the Deterministic Jitter parameter 
         1. Changed the typical spec from 10 ps to 15 ps 
         2. Removed max spec. 
      iii. Moved the Random Jitter parameter to the Outputs, Clocks (CML): CKOUTp, CKOUTn, CK16p, CK16n section and removed its max specification. 
   c. Updated Outputs, Clocks (CML): CKOUTp, CKOUTn, CK16p, CK16n section: 
      i. Update Rise and Fall Times parameter: 
         1. Changed the typical spec from 75 ps to 100 ps 
         2. Removed max spec. 
      ii. Removed min and max specs from Duty Cycle parameter. 
   d. Updated Output (LVCMOS/LVTTL): SYNC section: 
      i. Removed min and max specs for Output DC Resistance parameter. 
      ii. Updated Rise Time parameter: 
         1. Removed “\( C_L = 1 \text{ pF} \)” from Conditions 
         2. Changed typ spec from 50*\( C_L \) to 3.5 ns 
      iii. Updated Fall Time parameter: 
         1. Removed “\( C_L = 1 \text{ pF} \)” from Conditions 
         2. Changed typ spec from 3500*\( C_L \) to 0.05 ns 
   e. Updated SYNC Pulse Duration parameter: 
      i. Changed minimum spec from 21 ns to 32 cycles. 
   f. Updated Lock Time parameter:
i. Changed maximum spec from 152 cycles to 272 cycles.
g. Updated Footnotes
   i. Footnote # 2: changed “…RMS jitter measured on a 1010… pattern.” to “… RMS jitter measured on a clock pattern.”
   ii. Footnote # 3: changed “The rising and falling edges of the CK16 clock outputs…” to “The rising and falling edges of the CKOUT clock outputs…”

10. Updated MANRST section (page 9):
    a. Added sentence stating that MANRST resets the counter when input is low.
    b. Corrected the probability statistic within this paragraph from 0.625 to 0.0625.

11. Updated Timing Information section (page 13 – 15):
    a. Removed min and max specs in Half rate clock mode of operation table and Full rate clock mode of operation table (pages 13-14):
    b. Changed the max spec for the Lock Time parameter from 152 input clocks to 272 input clocks (page 15).

12. Updated QFN Pad Assignment table (page 20):
    a. Changed the signal name for pad #13 from “Test” to “NC” and modified the description.
    b. Changed “CLKSEL” description to remove reference to DMXSEL.
    c. Changed “MANRST” description by adding sentence stating that MANRST is active low.
    d. Added “Connect with external 5 kΩ pull up to VCCDA” wording in the “SYNC” description.

13. Updated the Order Information table: changed part number version from –S01 to –S02 (page 21).

14. Updated the Qualification Notification section, giving it a Limited status and associated wording, (page 21).

Version 2.0 to 2.1 (dated 2009-12-16):
1. Removed “Preliminary” watermark from document.
2. Updated Qualification Notice to indicate that the 1385DX-S02 is fully qualified.