The AppliedMicro APM86392 architecture provides the foundation for a new generation of flexible processing nodes required to satisfy the demands of intelligent all-IP networks and pervasive computing applications. The APM86392 architecture provides a platform whose components can play the role of various functions that operate today as single/multiple CPUs, ASICs, and/or FPGAs, for performance and power sensitive applications.

**Features**
- Dual-Core Power™ 465 processors each with a Floating Point Unit
- 32 KB I- and 32 KB D-cache L1
- 256 KB L2 cache per processor
- Hardware cache coherency
- DDR3 memory controller with optional ECC (36-bit)

**Offload Features**
- Security subsystem (optional) with acceleration for IPSec, SSL/TLS, SRTP/SRTCP, Kasumi, and public-key protocols (PKA)
- True Random Number Generator (TRNG)
- Ethernet Classification Engine
- Packet DMA
- SLIMpro acceleration / offload engine

**Queue Manager / Traffic Manager**
- Message passing architecture
- Manages 256 fixed size Queues

**High-Speed Interfaces**
- Two GE ports (RGMII) with Classification and TCP/IP off-load
- Three PCI Express® Gen 1/2 (x1) ports
- Two USB 2.0 Hosts with integrated PHYs
- One USB 2.0 OTG with integrated PHY
- One SATA 2.0 port

**Other Interfaces**
- Local Bus (EBUS)
- NAND Flash Controller
- Two I²C
- Four UARTs
- GPIOs
- Two SPI
- Two SDIO 3.0
- JTAG / Trace

**The Dual-Core IP Processor for Performance Applications**
The APM86392 PACKETpro™ architecture offers high-end processing performance. The innovative SoC subsystem design features the Scalable Lightweight Intelligent Management processor (SLIMpro) to enable breakthrough flexibility in power management, secure asymmetric multiprocessing (AMP), fail-over protection, resiliency, and end-to-end security for a wide range of applications from wired and wireless networking systems, to multi-function printers, industrial access points, and other mission-critical embedded systems.

At the heart of the APM86392 are two 1.0-GHz 465 processor cores based on Power™ Architecture with full SMP/AMP support and individual Floating Point processors. The Power cores are programmable through an industry-standard instruction set architecture (ISA). In addition, these processors are assisted by a rich set of configurable accelerators focused on packet classification, security, packet/data manipulation, and scheduling.

**465 Processor Complex Features**
The APM86392 incorporates two high performance 465 processors. Each 465 has five independent pipelines, a 32-KB data cache and a 32-KB instruction cache (which are 64-way set associative), and an IEEE floating point unit (FPU). Each of the 465 cores has a dedicated 256KB L2 cache with hardware cache coherency that attaches to the high-performance Processor Local Bus 5 (PLB5).

**Dedicated Ethernet Offload Engine**
In order to meet the needs of very low power and all-IP networks, the APM86392 includes a dedicated Ethernet Offload Engine. The Ethernet Offload Engine is capable of doing Inline IPsec with greater than 2-Gbps line rate throughput. It also provides for Inline TCP/IP and UDP checksums along with Energy Efficiency Ethernet capabilities (802.3az).

**Classification Engine**
The classification engine provides for flow, CoS, and port-based classification of data with 64-byte packet line-rate performance. It is programmable and can support IPv4, IPv6, and AppleTalk, as well as customer proprietary protocols.

**Queue Manager / Traffic Manager (QMTM)**
The Queue Manager / Traffic Manager is an important design consideration for the APM86392 and allows for the most efficient moving of packets/data between the processors and peripherals using a message passing architecture. This is accomplished through a central communication interface that offloads software from the routing of packets and from transaction synchronization.

The Queue Manager can be used to: centralize management of all transaction traffic, reduce communication overhead between software and hardware, and perform inter-processor message passing and work scheduling.

**SLIMpro – Power Management**
The APM86392 integrates a dedicated 32-bit SLIMpro accelerator processor that provides advanced capabilities such as dynamic power management and higher layer network acceleration. The SLIMpro processor leverages the APM86392 message passing architecture and other acceleration subsystems in order to provide application-specific processor offloads. It also provides advanced wake up capabilities from Deep Sleep Mode such as Wake on LAN, Wake on USB, Wake on PCIe, and Wake on Interrupts.
Advanced Security Engine
The APM86392 can deliver advanced security capabilities with the optional security engine. This security engine utilizes the QM4 for the fastest possible throughput between the 465 processor, memory, and the security engine itself. The security engine supports the following algorithms: DES, 3DES, AES, ARC-4 encryption, MD-5, SHA-1, SHA-256, and SHA-512 hashing with or without HMAC, Kasumi F8/ F9, and also includes acceleration for the following protocols: IPSec, SSL/TLS/DTLS, and SRTP/SRTCP. A true random number generator and a public key accelerator are also included.

Advanced DMA
The Packet DMA can be used to perform memory-to-memory transfers, which include the SDRAM, SRAM, PCIe, and EBUS memory spaces. Transfers can also include certain "on-the-fly" data manipulations such as: checksum generation or checking, CRC generation or checking, or XOR. The Packet DMA comprehends data packet delineation, which enables it to perform a comprehensive list of scatter/gather operations for packet assembly and disassembly with minimal software intervention.

APM86392 Partner Ecosystem
AppliedMicro’s APM86392 processors are supported by an extensive Partner ecosystem of products and services from a wide range of leading suppliers, including industry standard providers of:
- Embedded operating systems
- Hardware and software development tools
- Embedded software products and services
- Board-level products
- System design services
- Technical training

AppliedMicro offers an evaluation kit for product evaluation and for early software development.