With a processor speed of up to 1 GHz, support for floating-point operations, USB 2.0 OTG, PCI-Express, SATA, Gigabit Ethernet, security, NAND Flash interfaces, and low power dissipation, the AppliedMicro APM82181 embedded processor is ideally suited for next generation NAS applications that require exceptionally low power and a small footprint.

### Features

**Power™ 464 Processor Core**
- CPU Speed (frequency): 800 MHz and 1 GHz
- 7-stage pipeline, executes up to two instructions per cycle
- 32-KB-I/32-KB-D L1 caches, 64-way set-associative

**High-Performance Floating Point Unit**
- 5-stage FPU with 2.0 MFLOPS/MHz (SP/DP)
- Hardware support for IEEE 754
- Single-Precision and Double-Precision operation with thirty-two 64-bit floating-point registers
- Single cycle throughput on most instructions

**L2 Cache and On-Chip Memory**
- 256-KB L2/SRAM with parity protection
- 32-KB On-Chip Memory

**High-Bandwidth Bus Architecture**
- 128-bit processor local bus (PLB) with a two-way crossbar
- Separate 128-bit read and 128-bit write data bus for each way
- Up to 12.8 GB/s of peak on-chip bandwidth at 200 MHz

**DDR2 SDRAM**
- On-chip Double Data Rate 2 (DDR2) SDRAM controller with 32/16-bit interface
- Support for one rank of DDR2 SDRAM up to 512 MB

### APM82181 NAS Application Example
Features (cont’d)

Gen 1 PCI Express Interface
• One Gen1 x1 lane PCI-Express interface (2.5 GB/s per lane)
• Configurable as root or end-point

SATA
• Up to two SATA controllers operating at up to 3.0 GB/s each with integrated SERDES

RAID5
• On-chip RAID5 acceleration

Ethernet Port and TCP/IP Acceleration
• One Ethernet 10/100/1000-Mbit/s, full-duplex MAC (RGMII/MII)
• TCP/IP Acceleration Hardware and Jumbo Frame support

Turbo Security (Optional)
• On-chip IPSec/SSL acceleration with header/trailer processing
• Supports DES, 3DES, AES, ARC-4 encryption, MD-5, SHA-1, and SHA-256 hashing
• True and Pseudo random number generators (TRNG/PRNG)
• Public key accelerator (PKA)

USB 2.0 OTG Interface with Integrated PHY
• Operates at 1.5/12/480 Mbps

External Bus Interface
• Up to 100 MHz, 8-bit data bus external bus control (EBC) interface

NAND Flash Controller
• Supports one to three banks of NAND Flash memory devices
• Secure Boot using an on-chip 2-KB Boot ROM:
  • Initial Program Loader in 2-KB Boot ROM checks for ECC when copying block 0 to on-chip SRAM
• ECC generation - hamming code, single-bit correction, double-bit detection (SEC/DED):
  • ECC generation assist software with ECC checking of SLC NAND

Standard Peripherals
• On-chip real-time clock with external battery backup capability
• Up to two UARTs (1x 4-pin or 2x 2-pin)
• Two IIC (with one integrated boot strap controller)
• One SPI/SCP serial interface
• 32 General-Purpose I/O
• Support for JTAG board testing, JTAG debuggers, and 4xx instruction trace

For more information, visit http://www.appliedmicro.com

AppliedMicro Partners Ecosystem
• Extensive ecosystem of products and services from a wide range of leading suppliers
• For details of the products and services available, visit: http://www.appliedmicro.com/Embedded/Partners
• AppliedMicro also provides a reference design for this processor

Specifications

Technology
• 90nm CMOS

Performance (estimated)
• 1,600 Dhrystone 2.1 MIPS @ 800 MHz
• 2,000 Dhrystone 2.1 MIPS @ 1.0 GHz

Frequency
• CPU: Up to 1.0 GHz
• DDR2 Memory: 32/16-bit width
• PCI Express Gen 1
  • One 1-lane @ 2.5 Gbit/s per lane/direction
• SATA Controller
  • Up to two ports @ 1.5 or 3.0 Gb/s

Typical Power Dissipation
• 0.5 W (typical standby power)
• 2.4 W @ 800 MHz (typical operational power)

Case Temperature Range
• -20°C to +85°C

Power Supply
• 1.2 V (logic), 1.8 V (DDR2), 2.5 V (Ethernet, PCIe/SATA), 3.3 V (USB, other I/O)

Signal I/Os
• 189

Packaging
• Wirebond Fine-pitched Plastic BGA (345-pin FFBGA), 18 mm x 18 mm (0.8-mm ball pitch)
• RoHS compliant (lead-free)